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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
CHANG, ERIC	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 10/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/788,550	SONG, HO-UK	
	Examiner	Art Unit	
	Eric Chang	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4-5-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are pending.

Specification

2. The applicant or their representatives are urged to review the specification and submit corrections for all mistakes of a grammatical, clerical, or typographical nature. **For example**, on page 2, lines 6-13 of the specification contain numerous grammatical errors.

Claim Objections

3. Claims 6 and 14 are objected to because of the following informalities: the term "from1" on the last line of the claim should read, "from". Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 3, 11 and 19 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: in the limitation "the first predetermined timing is earlier one external clock period than the tRCD timing", the "earlier one external clock period" relationship is unclear.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-5 and 17-20 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by U.S. Patent Application Publication 2003/0090307A1 to Shin.

8. As to claim 1, Shin discloses an apparatus for controlling operations of a synchronous semiconductor memory device, wherein each operation is achieved by a plurality of internal instructions, comprising: a reference clock block [340] for receiving an external clock [PCLKDQ] and outputting a plurality of delayed clock signals [A, B, C, D]; and a control block [310], in response to the plurality of delayed clock signal, for outputting one of the plurality of internal instructions at a first predetermined timing which is earlier than the timing of starting the operation [paragraph 0015].

9. As to claim 2, Shin discloses an additive latency of the synchronous semiconductor memory device is not 0 [paragraph 0017].

10. As to claim 3, Shin discloses the first predetermined timing is earlier one external clock period than the tRCD timing [paragraph 0017].

11. As to claim 4, Shin discloses a synchronous memory device [paragraph 0004], and the plurality of delayed clock signals is used to control the delay of control signals such that data is outputted during an appropriate output time period [paragraph 0009]. It is well known in the art that control signals in the synchronous memory art include a clock delay signal, a CAS signal, a chip selecting signal, a write enable signal and a RAS signal.

12. As to claim 5, Shin discloses the outputted signal from the control block is for controlling the CAS latency [paragraph 0005]. By definition, the CAS determines decoding of an inputted column address signal.

13. As to claim 17, Shin discloses a method for controlling operations of a synchronous semiconductor memory device, wherein each operation is achieved by a plurality of internal instructions performing an instruction in response to an additive latency, comprising the step of: A) receiving an external clock [PCLKDQ] and outputting a plurality of delayed clock signals [A, B, C, D]; and B) outputting one of the plurality of internal instructions at a first predetermined timing which is earlier than the timing of starting the operation, in response to the plurality of delayed clock signal [paragraph 0015].

14. As to claim 18, Shin discloses an additive latency of the synchronous semiconductor memory device is not 0 [paragraph 0017].

15. As to claim 19, Shin discloses the first predetermined timing is earlier one external clock period than the tRCD timing [paragraph 0017].

16. As to claim 20, Shin discloses a synchronous memory device [paragraph 0004], and the plurality of delayed clock signals is used to control the delay of control signals such that data is outputted during an appropriate output time period [paragraph 0009]. It is well known in the art that control signals in the synchronous memory art include a clock delay signal, a CAS signal, a chip selecting signal, a write enable signal and a RAS signal.

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 6-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Publication 2003/0090307A1 to Shin, in view of Applicant's Admitted Prior Art.

19. As to claim 6, Shin teaches the limitations of the claim but does not specifically teach that an address controller, in response to one of the plurality of delayed clock signal, for outputting an inputted address signal at a second predetermined timing which is earlier than the timing of starting the operation; and a decoding block for decoding the outputted address signal from the address controller in response to the outputted signal from the control block.

Applicant's Admitted Prior Art teaches that a synchronous memory device has to compensate for CAS delay [page 2, lines 11-22]. Thus, Applicant's Admitted Prior Art teaches a synchronous memory device similar to that of Shin. Applicant's Admitted Prior Art further teaches an address controller, in response to one of the plurality of delayed clock signal, for outputting an inputted address signal at a second predetermined timing which is earlier than the timing of starting the operation [FIG. 3]; and a decoding block for decoding the outputted address signal from the address controller in response to the outputted signal from the control block [43].

At the time that the invention was made, it would have been obvious to a person of ordinary skill in the art to employ the address controller and decoder as taught by Applicant's Admitted Prior Art. One of ordinary skill in the art would have been motivated to do so that the address of the memory to be accessed could be properly decoded.

It would have been obvious to one of ordinary skill in the art to combine the teachings of the cited references because they are both directed to the problem of compensating for CAS delay in a synchronous memory device. Moreover, the output control means taught by Shin would improve the accuracy of Applicant's Admitted Prior Art because it prevents invalid output signals from being generated [paragraph 0012].

20. As to claim 7, Shin discloses the control block includes: a first transmission gate for outputting the decoded signal as the outputted signal when an additive latency is 0 or 1 [310]; first to fourth latches connected serially for sequentially latching the decoded signal [331, 332, 333, 334]; a second transmission gate for outputting the output signal of the second latch as the outputted signal when the additive latency is 2 [310]; and a third transmission gate for outputting the output signal of the fourth latch as the outputted signal when the additive latency is 3 [310]. Applicant's Admitted Prior Art teaches that the control block is used in an instruction decoder [43].

21. As to claim 8, Shin discloses the address controller includes: a first transmission gate for outputting the inputted address signal as the internal column address signal when the additive latency is 0 or 1 [310]; a first to fourth latches connected serially for sequentially latching the column address [331, 332, 333, 334]; a second transmission gate for outputting the output signal of the second latch as the internal column address when the additive latency is 2 [310]; and a third transmission gate for outputting the output signal of the fourth latch as the internal column address when the additive latency is 3 [310]. Applicant's Admitted Prior Art teaches that the control block is used in an address controller [FIG. 3].

22. As to claim 9, Applicant's Admitted Prior Art discloses a synchronous semiconductor memory device, comprising: an instruction and address receiving block for receiving an external clock, an external instruction, a row address and a column address and outputting a plurality of

internal instructions after decoding the external instruction [FIG. 1]; a row address control block, controlled by at least one of the plurality of internal instructions, for decoding the row address [31]; a column address control block, controlled by at least one of the plurality of internal instructions, for decoding the column address [41]; a bank for inputting or outputting a data in response to the decoded row and column addresses [32]; and an I/O block for delivering the data between the bank and an external circuit [80], wherein the column address control block includes a reference clock block [340] for receiving an external clock [PCLKDQ] and outputting a plurality of delayed clock signals [A, B, C, D]; and a control block [310], in response to the plurality of delayed clock signal, for outputting one of the plurality of internal instructions at a first predetermined timing which is earlier than the timing of starting the operation [paragraph 0015].

23. As to claim 10, Shin discloses an additive latency of the synchronous semiconductor memory device is not 0 [paragraph 0017].

24. As to claim 11, Shin discloses the first predetermined timing is earlier one external clock period than the tRCD timing [paragraph 0017].

25. As to claim 12, Shin discloses a synchronous memory device [paragraph 0004], and the plurality of delayed clock signals is used to control the delay of control signals such that data is outputted during an appropriate output time period [paragraph 0009]. It is well known in the art

that control signals in the synchronous memory art include a clock delay signal, a CAS signal, a chip selecting signal, a write enable signal and a RAS signal.

26. As to claim 13, Shin discloses the outputted signal from the control block is for controlling the CAS latency [paragraph 0005]. By definition, the CAS determines decoding of an inputted column address signal.

27. As to claim 14, Applicant's Admitted Prior Art discloses address controller, in response to one of the plurality of delayed clock signal, for outputting an inputted address signal at a second predetermined timing which is earlier than the timing of starting the operation [FIG. 3]; and a decoding block for decoding the outputted address signal from the address controller in response to the outputted signal from the control block [43].

28. As to claim 15, Shin discloses the control block includes: a first transmission gate for outputting the decoded signal as the outputted signal when an additive latency is 0 or 1 [310]; first to fourth latches connected serially for sequentially latching the decoded signal [331, 332, 333, 334]; a second transmission gate for outputting the output signal of the second latch as the outputted signal when the additive latency is 2 [310]; and a third transmission gate for outputting the output signal of the fourth latch as the outputted signal when the additive latency is 3 [310]. Applicant's Admitted Prior Art teaches that the control block is used in an instruction decoder [43].

29. As to claim 16, Shin discloses the address controller includes: a first transmission gate for outputting the inputted address signal as the internal column address signal when the additive latency is 0 or 1 [310]; a first to fourth latches connected serially for sequentially latching the column address [331, 332, 333, 334]; a second transmission gate for outputting the output signal of the second latch as the internal column address when the additive latency is 2 [310]; and a third transmission gate for outputting the output signal of the fourth latch as the internal column address when the additive latency is 3 [310]. Applicant's Admitted Prior Art teaches that the control block is used in an address controller [FIG. 3].

Conclusion

30. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Chang whose telephone number is (571) 272-3671. The examiner can normally be reached on M-F 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100